CLAIMS

What is claimed is.

1	1.	A process of forming a memory device, comprising:
2		forming a first topology over a substrate;
3		forming a subsequent topology over the first topology;
4		forming a first memory structure at the first topology; and
5		forming at least one subsequent memory structure at a corresponding at least one
6	subsec	quent topology.
1	2.	The process according to claim 1, wherein the memory device includes a
2	ferroelectric r	nemory device.
1	3.	The process according to claim 2, wherein forming at least one subsequent
2	memory struc	ture further includes:
3		forming a second topology;
4		forming a second memory structure at the second topology;
5		forming an interlayer dielectric (ILD) layer over the second memory structure;
6		forming a third topology above the ILD layer; and
7		forming a third memory structure at the third topology.
1	4.	The process according to claim 2, wherein forming at least one subsequent
2	memory struc	ture further includes:
3		forming a second topology;

5	memor	y structure is formed comprising:
6		forming a ferroelectric layer over the first memory structure;
7		forming a conductive layer over the layer;
8		planarizing the conductive layer; and
9		patterning the conductive layer to form a third electrode; and
10		forming an interlayer dielectric (ILD) layer over the second memory structure;
1 11		forming a third topology above the ILD layer; and
11 12 1 1 2 3 4		forming a third memory structure at the third topology.
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j j 1	5.	The process according to claim 2, wherein forming a first memory structure
2 13 2	further include	s:
3		forming a first electrode over the substrate;
4		forming a first memory layer over the first electrode; and
5		forming a second electrode over the first memory layer.
1	6.	The process according to claim 2, wherein forming a first memory structure and
2	forming a subs	equent memory structure further includes:
3		forming a first electrode over the substrate;
4		forming a first memory layer over the first electrode;
5		forming a second electrode over the first memory layer;

forming a second memory structure at the second topology, wherein the second

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forming a second memory layer over the second electrode; and

forming a third electrode over the second memory layer.

1	7.	A process of forming a ferroelectric polymer memory device, comprising:
2		forming a first topology above a substrate;
3		forming a subsequent topology over the first topology;
4		forming a first ferroelectric polymer memory structure at the first topology; and
5		forming at least one subsequent ferroelectric polymer memory structure at a
6	corres	ponding at least one subsequent topology.
1	8.	The process according to claim 7, wherein forming a subsequent ferroelectric
2	polymer mem	nory structure further comprises:
3		forming a second topology;
4		forming a second ferroelectric polymer memory structure at the second topology;
5		forming an interlayer dielectric (ILD) layer over the second ferroelectric polymer
6	memo	ry structure;
7		forming a third topology above the ILD layer; and
8		forming a third ferroelectric polymer memory structure at the third topology.
1	9.	The process according to claim 7, wherein forming a subsequent ferroelectric
2	polymer mem	ory structure further comprises:
3		forming a second topology;
4		forming a second ferroelectric polymer memory structure at the second topology,
5	where	in the second ferroelectric polymer memory structure is formed comprising:

0		forming a ferroelectric polymer layer over the first ferroelectric polymer
7		memory structure;
8		forming a conductive layer over the ferroelectric polymer layer;
9		planarizing the conductive layer; and
10		patterning the conductive layer to form a third electrode; and
11		forming an interlayer dielectric (ILD) layer over the second ferroelectric polymer
12	memo	ory structure;
13		forming a third topology above the ILD layer; and
14		forming a third ferroelectric polymer memory structure at the third topology.
1	10.	The process according to claim 7, wherein forming a first ferroelectric memory
2	structure furtl	her comprises:
3		forming a first electrode over the substrate;
4		forming a first ferroelectric memory layer over the first electrode; and
5		forming a second electrode over the first ferroelectric memory layer.
1	11.	The process of forming a memory device according to claim 7, wherein forming a
2	first ferroelec	tric polymer memory structure and forming a subsequent ferroelectric polymer
3	memory struc	ture further comprises:
4		forming a first electrode over the substrate;
5		forming a first ferroelectric polymer memory layer over the first electrode;
6		forming a second electrode over the first ferroelectric polymer memory layer;

7		forming a second ferroelectric polymer memory layer over the second electrode;
8	and	
9		forming a third electrode over the second ferroelectric polymer memory layer.
1	12.	The process of forming a polymer memory device according to claim 7, wherein
2	forming a ferr	oelectric polymer memory structure comprises forming a layer selected from spin
3	on depositing	, chemical vapor depositing, substrate dip depositing, Langmuir-Blodgett
4	depositing, an	nd spray-on depositing.
1	13.	A process of forming a ferroelectric oxide memory device, comprising:
2		forming a first topology above a substrate;
3		forming a subsequent topology over the first topology;
4		forming a first ferroelectric oxide memory structure at the first topology; and
5		forming at least one subsequent ferroelectric oxide memory structure at a
6	corres	eponding at least one subsequent topology.
1	14.	The process according to claim 13, wherein forming a subsequent ferroelectric
2	oxide memor	y structure further comprises:
3		forming a second topology;
4		forming a second ferroelectric oxide memory structure at the second topology;
5		forming an interlayer dielectric (ILD) layer over the second ferroelectric oxide
6	memo	ory structure;
7		forming a third topology above the ILD layer; and

1	15.	The process according to claim 13, wherein forming a subsequent ferroelectric
2	oxide memory	structure further comprises:
3		forming a second topology;
4		forming a second ferroelectric oxide memory structure at the second topology,
5	wherei	n the second ferroelectric oxide memory structure is formed comprising:
6		forming a ferroelectric oxide layer over the first ferroelectric oxide
7		memory structure;
8		forming a conductive layer over the ferroelectric oxide layer;
9		planarizing the conductive layer; and
10		patterning the conductive layer to form a third electrode; and
11		forming an interlayer dielectric (ILD) layer over the second ferroelectric oxide
12	memo	ry structure;
13		forming a third topology above the ILD layer; and
14		forming a third ferroelectric oxide memory structure at the third topology.
1	16.	The process according to claim 13, wherein forming a first ferroelectric oxide
2	memory struc	ture further comprises:
3		forming a first electrode over the substrate;
4		forming a first ferroelectric oxide memory layer over the first electrode; and
5		forming a second electrode over the first ferroelectric oxide memory layer.

forming a third ferroelectric oxide memory structure at the third topology.

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1	17.	The process of forming a memory device according to claim 13, wherein forming	
2	a first ferroele	ectric oxide memory structure and forming a subsequent ferroelectric oxide memory	
3	structure further comprises:		
4		forming a first electrode over the substrate;	
5		forming a first ferroelectric oxide memory layer over the first electrode;	
6		forming a second electrode over the first ferroelectric oxide memory layer;	
7		forming a second ferroelectric oxide memory layer over the second electrode; and	
8		forming a third electrode over the second ferroelectric oxide memory layer.	
1	18.	The process according to claim 13, wherein forming a ferroelectric oxide memory	
2	structure com	prises forming a layer selected from chemical vapor deposition, spin-on deposition,	
3	and physical v	vapor deposition.	
1	19.	A ferroelectric memory device comprising:	
2		a first topology disposed over a substrate;	
3		a first ferroelectric structure disposed in the first topology; and	
4		a subsequent topology disposed over the first topology, and a subsequent	
5	ferroe	lectric structure disposed in the subsequent topology.	
1	20.	The ferroelectric memory device according to claim 19, wherein the first	
2	ferroelectric s	tructure and a subsequent ferroelectric structure further comprise:	
3		a first electrode disposed over the substrate;	
4		a first ferroelectric polymer layer disposed over the first electrode;	

5		a second electrode disposed over the first ferroelectric polymer layer;
6		a second ferroelectric polymer layer disposed over the second electrode; and
7	a thire	d electrode disposed over the second ferroelectric polymer layer.
1	21.	The ferroelectric memory device according to claim 20, wherein the electrodes
2	have a width	that is a minimum feature of a photolithography technology, selected from 0.25
3	micron, 0.18 micron, 0.13 micron, and 0.11 micron.	
1	22.	The ferroelectric memory device according to claim 20, wherein the first
2	ferroelectric s	structure and a subsequent ferroelectric structure further comprise:
3		a first electrode disposed over the substrate;
4		a first ferroelectric oxide layer disposed over the first electrode;
5		a second electrode disposed over the first ferroelectric oxide layer;
6		a second ferroelectric oxide layer disposed over the second electrode; and
7		a third electrode disposed over the second ferroelectric oxide layer.
1	23.	The ferroelectric memory device according to claim 21, wherein the electrodes
2	have a width	that is a minimum feature of a photolithography technology, selected from 0.25
3	micron, 0.18	micron, 0.13 micron, and 0.11 micron.
1	24.	A system, comprising:
2		a processor;

a ferroelectric memory system coupled to the processor;

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4		an input/output (I/O) circuit coupled to the processor and the ferroelectric
5	meme	ory system; and
6		the ferroelectric memory system including:
7		a substrate;
8		a first topology disposed over the substrate;
9		a first ferroelectric structure disposed in the first topology; and
0		a subsequent topology disposed over the first topology, and a subsequent
1		ferroelectric structure disposed in the subsequent topology.
1	25.	The system according to claim 24, wherein the processor is disposed in a host
2	selected from	a clock, a television, a cell phone, a personal computer, an automobile, an
3	industrial con	ntrol system, and an aircraft.
1	26.	The system according to claim 24, wherein the ferroelectric memory structure is
2	selected from	a ferroelectric polymer memory structure and a ferroelectric oxide memory
3	structure.	
1	27.	The system according to claim 24, wherein the processor comprises a CMOS

die in a memory module.

logic region disposed in the substrate, and wherein the ferroelectric memory system comprises a

- 1 28. The system according to claim 24, wherein the processor comprises logic in a
- 2 memory controller, and wherein the ferroelectric memory system comprises a die in a memory
- 3 module.
- 1 29. The system according to claim 24, wherein the ferroelectric memory system
- 2 comprises a chip in a chipset.